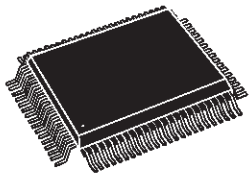
ST92R195B

ROMLESS HCMOS MCU WITH ON-SCREEN-DISPLAY AND TELETEXT DATA SLICER

DATA BRIEFING

- Register File based 8/16 bit Core Architecture with RUN, WFI, SLOW and HALT modes
- 0°C to +70°C Operating Temperature Range available
- Up to 24 MHz Operation @ 5V±10%
- Minimum instruction cycle time: 375ns at 16 MHz internal clock
- 4 Mbytes address space
- 256 Bytes RAM of Register file (accumulators or index registers)
- 1024 Bytes of on-chip static RAM
- 8K Bytes of TDSRAM (Teletext and Display Storage RAM)
- 80-lead QFP package
- 23 fully programmable I/O pins
- Serial Peripheral Interface
- Flexible Clock controller for OSD, Data Slicer and Core clocks running from one single low frequency external crystal.
- Enhanced Display Controller with 26 rows of 40/80 characters
  - Serial and Parallel attributes
  - 10x10 dot Matrix, 512 ROM characters, definable by user
  - 4/3 and 16/9 supported in 50/60Hz and 100/120 Hz mode
  - Rounding, fringe, double width, double height, scrolling, cursor, full background color, half-intensity color, translucency and half-tone modes
- Teletext unit, including Data slicer, Acquisition Unit and 8 Kbytes TDSRAM for Data Storage
- VPS and Wide Screen Signalling slicer
- Integrated Sync Extractor and Sync Controller
- 14-bit Voltage Synthesis for tuning reference voltage
- Up to 8 External Interrupts plus 1 non-maskable interrupt



QFP80

- 8 x 8-bit programmable PWM outputs with 5V open-drain or push-pull capability
- 16-bit Watchdog timer with 8-bit prescaler
- One 16-bit standard timer with 8-bit prescaler
- 4-channel Analog-to-Digital converter; 5-bit guaranteed
- Rich instruction set and 14-Addressing modes

Versatile Development Tools, including Assembler, Linker, C-compiler, Archiver, Source Level Debugger and Hardware Emulators with Real-Time Operating System available from third parties

Device Summary

Device	Program Memory	TDS RAM	VPS/ WSS	Package
ST92R195B9	ROMLESS	8K	Yes	PQFP80

Rev. 2.2

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST92R195B microcontroller is developed and manufactured by STMicroelectronics using a proprietary n-well HCMOS process. Its performance derives from the use of a flexible 256-register programming model for ultra-fast context switching and real-time event response. The intelligent on-chip peripherals offload the ST9 core from I/O and data management processing tasks allowing critical application tasks to get the maximum use of core resources. The ST92R195B MCU supports low power consumption and low voltage operation for power-efficient and low-cost embedded systems.

1.1.1 ST9+ Core

The advanced Core consists of the Central Processing Unit (CPU), the Register File and the Interrupt controller.

The general-purpose registers can be used as accumulators, index registers, or address pointers. Adjacent register pairs make up 16-bit registers for addressing or 16-bit processing. Although the ST9 has an 8-bit ALU, the chip handles 16-bit operations, including arithmetic, loads/stores, and memory/register and memory/memory exchanges.

Two basic addressable spaces are available: the Memory space and the Register File, which includes the control and status registers of the on-chip peripherals.

1.1.2 Power Saving Modes

To optimize performance versus power consumption, a range of operating modes can be dynamically selected.

Run Mode. This is the full speed execution mode with CPU and peripherals running at the maximum clock speed delivered by the Phase Locked Loop (PLL) of the Clock Control Unit (CCU).

Wait For Interrupt Mode. The Wait For Interrupt (WFI) instruction suspends program execution until an interrupt request is acknowledged. During WFI, the CPU clock is halted while the peripheral and interrupt controller keep running at a frequency programmable via the CCU. In this mode, the power consumption of the device can be reduced by more than 95% (LP WFI).

Halt Mode. When executing the HALT instruction, and if the Watchdog is not enabled, the CPU and its peripherals stop operating and the status of the machine remains frozen (the clock is also stopped). A reset is necessary to exit from Halt mode.

1.1.3 I/O Ports

Up to 23 I/O lines are dedicated to digital Input/ Output. These lines are grouped into up to five I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer and output, analog inputs, external interrupts and serial or parallel I/O.

1.1.4 TV Peripherals

A set of on-chip peripherals form a complete system for TV set and VCR applications:

– Voltage Synthesis

– VPS/WSS Slicer

– Teletext Slicer

– Teletext Display RAM

– OSD

1.1.5 On Screen Display

The human interface is provided by the On Screen Display module, this can produce up to 26 lines of up to 80 characters from a ROM defined 512 character set. The character resolution is 10x10 dots. Four character sizes are supported. Serial attributes allow the user to select foreground and background colours, character size and fringe background. Parallel attributes can be used to select additional foreground and background colors and underline on a character by character basis.

1.1.6 Teletext and Display RAM

The internal 8k Teletext and Display storage RAM can be used to store Teletext pages as well as Display parameters.

INTRODUCTION (Cont'd)

1.1.7 Teletext, VPS and WSS Data Slicers

The three on-board data slicers using a single external crystal are used to extract the Teletext, VPS and WSS information from the video signal. Hardware Hamming decoding is provided.

1.1.8 Voltage Synthesis Tuning Control

14-bit Voltage Synthesis using the PWM (Pulse Width Modulation)/BRM (Bit Rate Modulation) technique can be used to generate tuning voltages for TV set applications. The tuning voltage is output on one of two separate output pins.

1.1.9 PWM Output

Control of TV settings is able to be made with up to eight 8-bit PWM outputs, with a frequency maximum of 23,437Hz at 8-bit resolution (INTCLK = 12 MHz). Low resolutions with higher frequency operation can be programmed.

1.1.10 Serial Peripheral Interface (SPI)

The SPI bus is used to communicate with external devices via the SPI, or I C bus communication standards. The SPI uses a single line for data input and output. A second line is used for a synchronous clock signal.

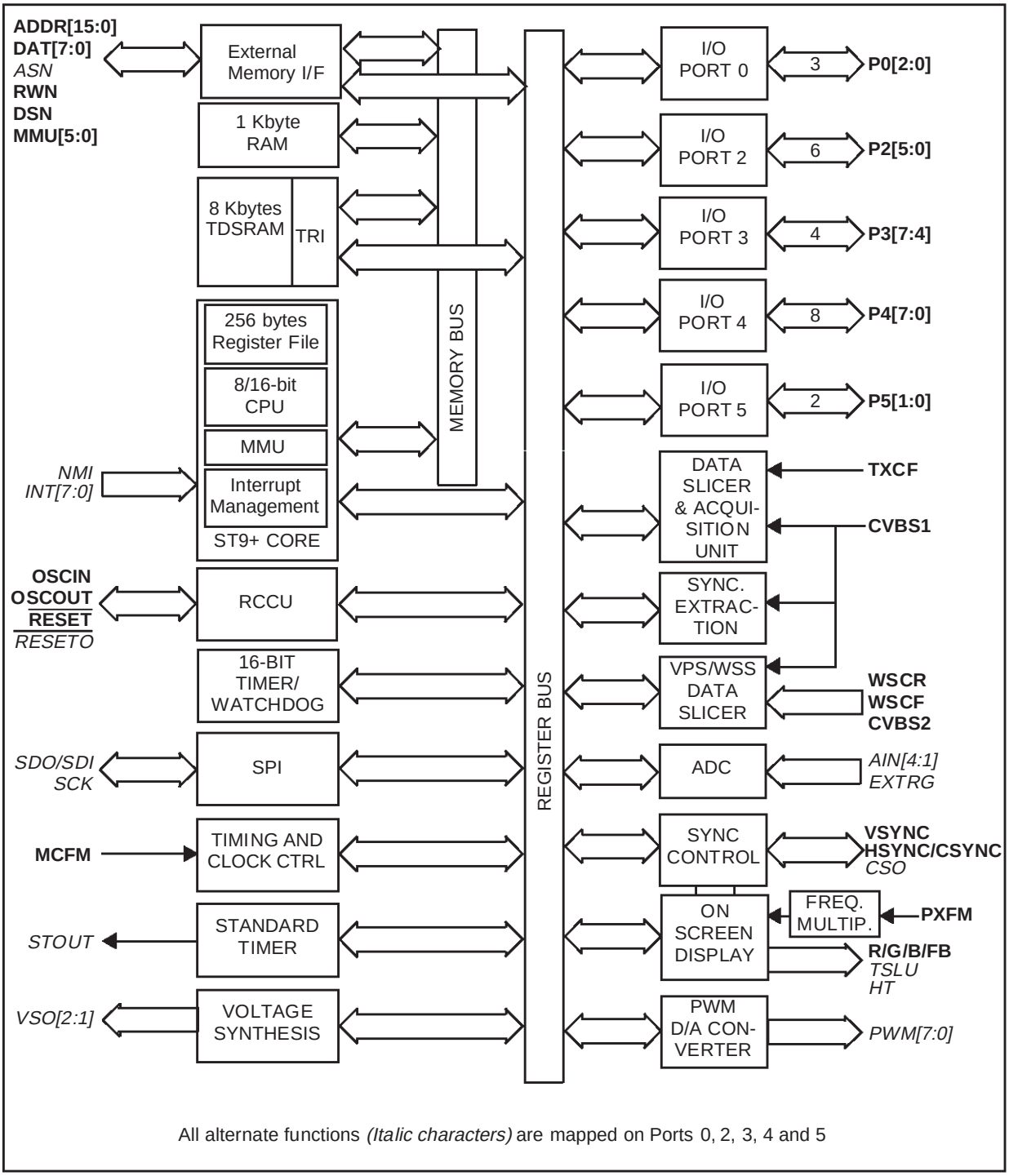
1.1.11 Standard Timer (STIM)

The ST92R195B has one Standard Timer that includes a programmable 16-bit down counter and an associated 8-bit prescaler with Single and Continuous counting modes.

1.1.12 Analog/Digital Converter (ADC)

In addition there is a 4 channel Analog to Digital Converter with integral sample and hold, fast 5.75µs conversion time and 6-bit guaranteed resolution.

Figure 1. ST92R195B Block Diagram



All alternate functions *(Italic characters)* are mapped on Ports 0, 2, 3, 4 and 5

1.2 PIN DESCRIPTION

ADDR[15:0] External memory interface address bus.

CVBS1 Composite video input signal for the Teletext slicer and sync extraction.

CVBS2 Composite video input signal for the VPS/WSS slicer. Pin AC coupled.

CVBSO, JTDO, JTCK Test pins: leave floating.

DAT[7:0] External memory interface data bus.

DSN Data strobe for external memory interface.

FB *Fast Blanking*. Video analog DAC output.

GND Digital circuit ground.

GNDA Analog circuit ground (must be tied externally to digital GND).

GNDM External memory interface ground.

HSYNC/CSYNC *Horizontal/Composite sync*. Horizontal or composite video synchronisation input to OSD. Positive or negative polarity.

JTRST0 Test pin: must be tied to GND.

MCFM Analog pin for the display pixel frequency multiplier.

MMU[5:0] External memory interface MMU segment bus

OSCIN, OSCOUT *Oscillator* (input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

PXFM Analog pin for the Display Pixel Frequency Multiplier

$\overline{\text{RESET}}$ *Reset* (input, active low). The ST9+ is initialised by the Reset signal. With the deactivation of RESET, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

R/G/B *Red/Green/Blue*. Video color analog DAC outputs.

RWN Read/Write strobe for external memory interface.

TEST0 Test pin: must be tied to V_{DDA}.

TXCF Analog pin for the teletext PLL.

V_{DD} Main power supply voltage (5V ±10%, digital)

V_{DDA} Analog power supply (must be tied externally to V_{DDA}).

V_{DDM} External memory interface power supply.

VSYNC *Vertical Sync*. Vertical video synchronisation input to OSD. Positive or negative polarity.

WSCF, WSCR Analog pins for the VPS/WPP slicer. These pins must be tied to ground or not connected.

P0[2:0], P2[5:0], P3[7:4], P4[7:0], P5[1:0]- *I/O Port Lines* (Input/Output, TTL or CMOS compatible). 23 lines grouped into I/O ports, bit programmable as general purpose I/O or as Alternate functions (see I/O section).

Important: Note that open-drain outputs are for logic levels only and are not true open drain.

1.2.1 I/O Port Alternate Functions.

Each pin of the I/O ports of the ST92R195B may assume software programmable Alternate Functions as shown in the Pin Configuration drawings. Table 1. shows the Functions allocated to each I/O Port pin.

Figure 2. 80-Pin Package Pin-Out

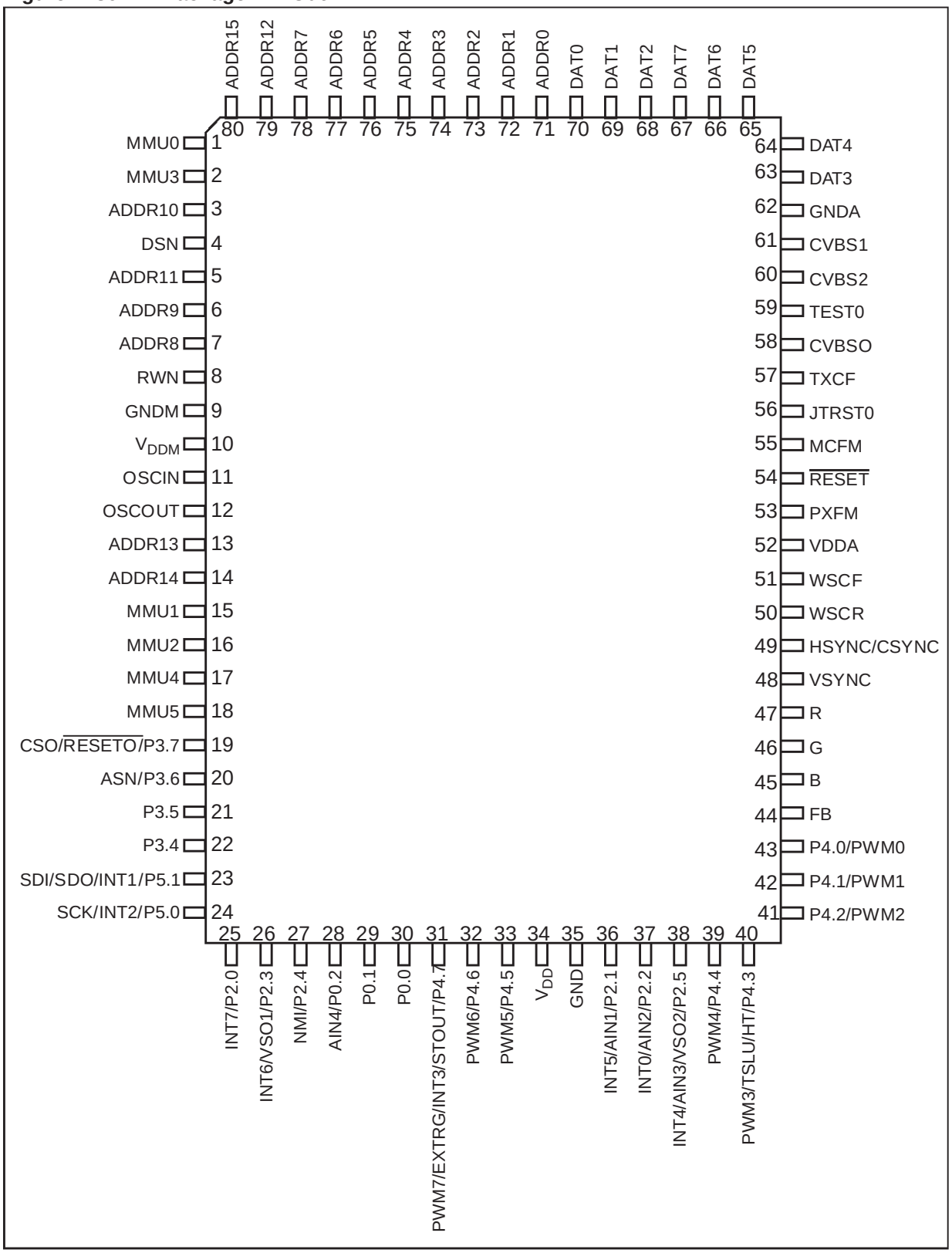


Table 1. ST92R195B I/O Port Alternate Function

Port Name	General Purpose I/O	Pin No. PQFP80	Alternate Functions		
P0.0	All ports useable for general purpose I/O (input, output or bidirectional)	30		I/O	
P0.1		29		I/O	
P0.2		28	AIN4	I	A/D Analog Data Input 4
P2.0		25	INT7	I	External Interrupt 7
P2.1		36	AIN1	I	A/D Analog Data Input 1
			INT5	I	External Interrupt 5
P2.2		37	INT0	I	External Interrupt 0
			AIN2	I	A/D Analog Data Input 2
P2.3		26	INT6	I	External Interrupt 6
			VSO1	O	Voltage Synthesis Output 1
P2.4		27	NMI	I	Non Maskable Interrupt Input
P2.5		38	AIN3	I	A/D Analog Data Input 3
			INT4	I	External Interrupt 4
			VSO2	O	Voltage Synthesis Output 2
P3.4		22		I/O	
P3.5		21		I/O	
P3.6		20	ASN	O	External Memory Interface Address Strobe
P3.7		19	RESET0	O	Internal Reset Output
			CSO	O	Composite Sync output
P4.0		43	PWM0	O	PWM Output 0
P4.1		42	PWM1	O	PWM Output 1
P4.2		41	PWM2	O	PWM Output 2
P4.3		40	PWM3	O	PWM Output 3
			TSLU	O	Translucency Digital Output
			HT	O	Half-tone Output
P4.4		39	PWM4	O	PWM Output 4
P4.5		33	PWM5	O	PWM Output 5
P4.6		32	PWM6	O	PWM Output 6
P4.7		31	EXTRG	I	A/D Converter External Trigger Input
			PWM7	O	PWM Output 7
			STOUT	O	Standard Timer Output
			INT3	I	External Interrupt 3
P5.0		24	INT2	I	External Interrupt 2
			SCK	O	SPI Serial Clock
P5.1		23	SDO	O	SPI Serial Data Out
			SDI	I	SPI Serial Data In
			INT1	I	External Interrupt 1

PIN DESCRIPTION (Cont'd)

1.2.2 I/O Port Styles

Pins	Physical Pull-Up	Pin Style	Reset Values
P0[2:0]	no	standard I/O	BID / OD / TTL
P2[5,4,3,2]	no	standard I/O	BID / OD / TTL
P2[1:0]	no	std I/O, trigger	BID / OD / TTL
P3.7	yes	standard I/O	AF / PP / TTL
P3[6,5,4]	no	standard I/O	BID / OD / TTL
P4[7:0]	no	standard I/O	BID / OD / TTL
P5[1:0]	no	standard I/O	BID / OD / TTL

Legend:

AF= Alternate Function, BID = Bidirectional, OD = Open Drain

PP = Push-Pull, TTL = TTL Standard Input Levels

How to Read this Table

To configure the I/O ports, use the information in this table and the Port Bit Configuration Table in the I/O Ports Chapter of the datasheet.

Port Style= the hardware characteristics fixed for each port line.

Inputs:

– If port style = Standard I/O, either TTL or CMOS input level can be selected by software.

– If port style = Schmitt trigger, selecting CMOS or TTL input by software has no effect, the input will always be Schmitt Trigger.

Weak Pull-Up = This column indicates if a weak pull-up is present or not.

– If WPU = yes, then the WPU can be enabled/disable by software

– If WPU = no, then enabling the WPU by software has no effect

Alternate Functions (AF) = More than one AF cannot be assigned to an external pin at the same time:

An alternate function can be selected as follows.

AF Inputs:

– AF is selected implicitly by enabling the corresponding peripheral. Exception to this are ADC analog inputs which must be explicitly selected as AF by software.

AF Outputs or Bidirectional Lines:

– In the case of Outputs or I/Os, AF is selected explicitly by software.

Example 1: ADC trigger digital input

AF: EXTRG, Port: P4.7, Port Style: Standard I/O.

Write the port configuration bits (for TTL level):

P4C2.7=1

P4C1.7=0

P4C0.7=1

Enable the ADC trigger by software as described in the ADC chapter.

Example 2: PWM 0 output

AF: PWM0, Port: P4.0

Write the port configuration bits (for output push-pull):

P4C2.0=0

P4C1.0=1

P4C0.0=1

Example 3: ADC AIN1 analog input

AF: AIN1, Port : P2.1, Port style: does not apply to analog inputs

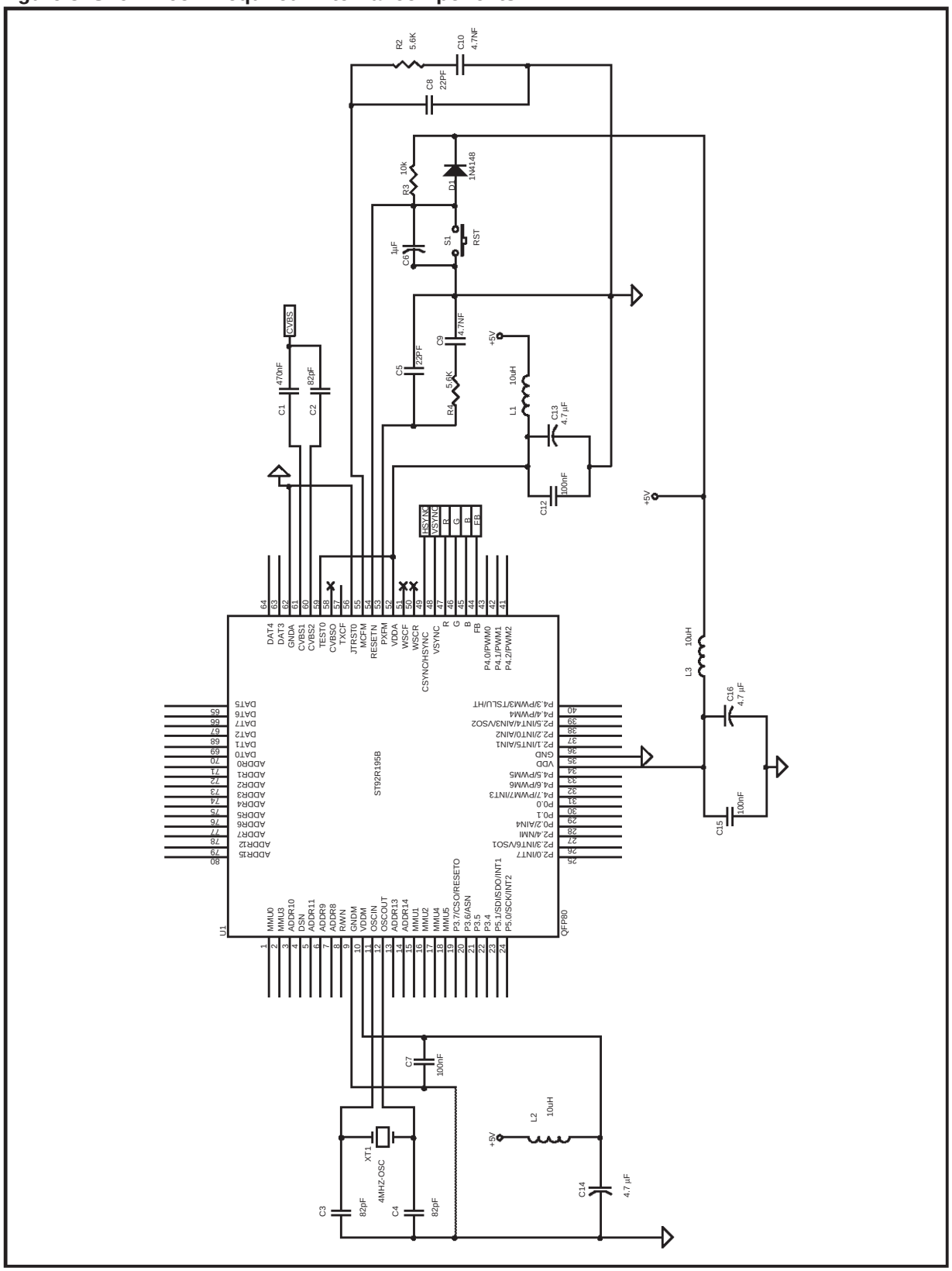
Write the port configuration bits:

P2C2.1=1

P2C1.1=1

P2C0.1=1

Figure 3. ST92R195B Required External components



1.3 MEMORY MAP

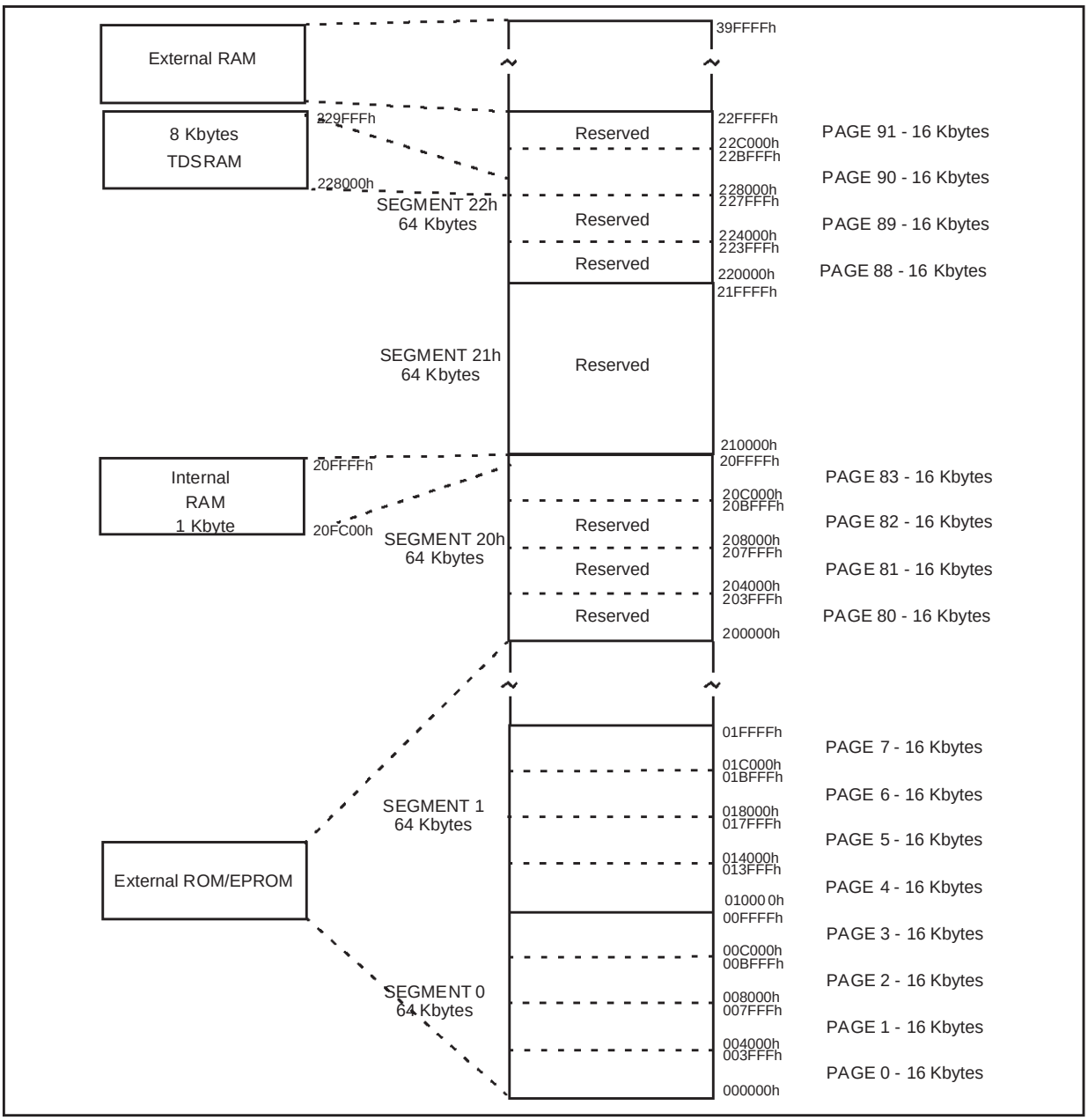
No Internal ROM

Internal RAM, 1 Kbytes
The internal RAM is mapped in MMU segment 20h; from address FC00h to FFFFh.

Internal TDSRAM, 8K bytes expandable up to 16K (into segment 22h)
The Internal TDSRAM is mapped into the MMU segment 22h. The TDSRAM is a fully static memory.

The TDSRAM is an 8K bytes mapped at the address 8000h to 9FFFh.

Figure 4. ST92R195B Memory Map



2 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	V_{SS} - 0.3 to V_{SS} + 7.0	V
V_{SSA}	Analog Ground	V_{SS} - 0.3 to V_{SS} + 0.3	V
V_{DDA}	Analog Supply Voltage	V_{DD} -0.3 to V_{DD} +0.3	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} +0.3	V
V_{AI}	Analog Input Voltage (A/D Converter)	V_{SS} - 0.3 to V_{DD} +0.3 V_{SSA} - 0.3 to V_{DDA} +0.3	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
T_{STG}	Storage Temperature	- 55 to + 150	°C
I_{INJ}	Pin Injected Current Maximum Accumulated Pin Injected Current In Device	- 5 to + 5 - 50 to +5 0	mA mA

Note: Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	0	70	°C
V_{DD}	Supply Voltage	4.5	5.5	V
V_{DDA}	Analog Supply Voltage (PLL)	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency	3.3	8.7	MHz
f_{OSCI}	Internal Clock Frequency (INTCLK)		24	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Value		Unit
			Min.	Max.	
V_{IHCK}	Clock in high level	external clock	0.7 V_{DD}		V
V_{ILCK}	Clock in low level	external clock		0.3 V_{DD}	V
V_{IH}	Input high level	TTL	2.0		V
V_{IL}	Input low level	TTL		0.8	V
V_{IH}	Input high level	CMOS	0.8 V_{DD}		V
V_{IL}	Input low level	CMOS		0.2 V_{DD}	V
V_{IHRS}	Reset in high level		0.7 V_{DD}		V
V_{ILRS}	Reset in low level			0.3 V_{DD}	V
V_{HYRS}	Reset in hysteresis		0.3		V
V_{IHY}	P2.(1:0) input hysteresis		0.9		V
V_{IHVH}	HSYNC/VSYNC input high level		0.7 V_{DD}		V
V_{ILVH}	HSYNC/VSYNC input low level			0.3 V_{DD}	V
V_{HYHV}	HSYNC/VSYNC input hysteresis		0.5		V
V_{OH}	Output high level	Push-pull Ild=-0.8mA	V_{DD}-0.8		V
V_{OL}	Output low level	Push-pull Id=+1.6mA		0.4	V
I_{WPU}	Weak pull-up current	bidir. state V_{OL}= 3V V_{OL}= 7V	50	 350	µA
I_{LKIO}	I/O pin input leakage current	$0<V_{IN}<V_{DD}$	-10	+10	µA
I_{LKRS}	Reset pin input	$0<V_{IN}<V_{DD}$	-10	+10	µA
I_{LKAD}	A/D pin input leakage current	alternate funct. op. drain	-10	+10	µA
I_{LKOS}	OSCIN pin input leakage current	$0<V_{IN}<V_{DD}$	-10	+10	µA

AC ELECTRICAL CHARACTERISTICS

PIN CAPACITANCE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified))

Symbol	Parameter	Conditions	Value		Unit
			min	max	
C_{IO}	Pin Capacitance Digital Input/Output			10	pF

CURRENT CONSUMPTION

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified)

Symbol	Parameter	Conditions	Value			Unit
			min	typ.	max	
I_{DD1}	Run Mode Current	notes 1,2; all On		70	100	mA
I_{DDA1}	Run Mode Analog Current (pin V_{DDA})	Timing Controller On		35	50	mA
I_{DD2}	HALT Mode Current	notes 1,4		10	100	µA
I_{DDA2}	HALT Mode Analog Current (pin V_{DDA})	notes 1,4		40	100	µA

Notes:

1. Port 0 is configured in push-pull output mode (output is high). Ports 2, 3, 4 and 5 are configured in bi-directional weak pull-up mode resistor. The external CLOCK pin (OSCIN) is driven by a square wave external clock at 8 MHz. The internal clock prescaler is in divide-by-1 mode.
2. The CPU is fed by a 24 MHz frequency issued by the Main Clock Controller. VSYNC is tied to V_{SS}, HSYNC is driven by a 15625Hz clock. All peripherals working including Display.
3. The CPU is fed by a 24 MHz frequency issued by the Main Clock Controller. VSYNC is tied to V_{SS}, HSYNC is driven by a 15625Hz clock. The TDSRAM interface and the Slicers are working; the Display controller is not working.
4. VSYNC and HSYNC tied to V_{SS}. External CLOCK pin (OSCIN) is held low. All peripherals are disabled.

EXTERNAL INTERRUPT TIMING TABLE (rising or falling edge mode)

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified))

Symbol	Parameter	Conditions	Value		Unit
		INTCLK=24 MHz.	min	max	
T_{wLR}	Low level pulse width	TpC+12	95		ns
T_{wHR}	High level pulse width	TpC+12	95		ns

TpC is the INTCLK clock period.

AC ELECTRICAL CHARACTERISTICS (Cont'd)

EXTERNAL MEMORY INTERFACE TIMING TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified))

Symbol	Parameter	Value		Unit
		typ	max	
T_{wDSR}	DSN low level pulse width (read)	TpC*(1/2+WDS)-6		ns
T_{wDSW}	DSN low level pulse width (write)	TpC*(1/2+WDS)-6		ns
T_{dDSR}(DR)	DSN↓ to data valid delay	TpC*(1/2+WDS)-16		ns
T_{hDR}(DS)	Data to DSN↑ hold time	0		ns
T_{dDS}(A)	DSN↑ to address active delay	TpC/2		ns
T_{hDS}(AS)	DSN↑ to ASN↓ delay	TpC/2 + 6		ns
T_{sRW}(AS)	R/WN setup time before ASN↑	TpC*(1/2 + WAS) - 8		ns
T_{dDSR}(RW)	DSN↑ to R/WN and address not valid delay	TpC/2		ns
T_{dDW}(DSW)	Write data valid to DSN↓ delay (write)	0		ns
T_{hDS}(DW)	Data hold time after DSN↑ (write)	TpC/2		ns
T_{dA}(DR)	Address valid to data valid delay (read)	TpC*(3/2+WDS+WAS)-14		ns

TpC is the INTCLK clock period.

SPI TIMING TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; Cload= 50pF)

Symbol	Parameter	Condition	Value		Unit
			min	max	
T_{sDI}	Input Data Set-up Time		tbd		ns
T_{hDI}	Input Data Hold Time (1)	OSCIN/2 as internal Clock	1INTCLK	+100ns	ns
T_{dOV}	SCK to Output Data Valid			tbd	ns
T_{hDO}	Output Data Hold Time		tbd		ns
T_{wSKL}	SCK Low Pulse Width		tbd		ns
T_{wSKH}	SCK High Pulse Width		tbd		ns

(1) TpC is the OSCIN clock period; TpMC is the "Main Clock Frequency" period.

SKEW CORRECTOR TIMING TABLE

(V_{DD}= 5V +/-10%, T_A= 0 to 70°C, unless otherwise specified)

Symbol	Parameter	Conditions	max Value	Unit
T_{jskw}	Jitter on RGB output	36 MHz Skew corrector clock frequency	5*	ns

(*) The OSD jitter is measured from leading edge to leading edge of a single character row on consecutive TV lines. The value is an envelope of 100 fields

AC ELECTRICAL CHARACTERISTICS (Cont'd)

OSD DAC CHARACTERISTICS

(V_{DD}= 5V +/-10%, T_A= 0 to 70°C, unless otherwise specified).

Symbol	Parameter	Conditions	Value			Unit
			min	typical	max	
	Output impedance: FB,R,G,B		300	500	700	Ohm
	Output voltage: FB,R,G,B	Cload= 20pF RL = 100K				
	code= 111			1.000		V
	code= 011			0.459	0.509	V
	code= 000			0.025	0.050	V
	FB= 1		2.4	3.0	4.0	V
	FB= 0		0	0.025	0.050	V
	Global voltage accuracy				+/-5	%

A/D CONVERTER, EXTERNAL TRIGGER TIMING TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified

Symbol	Parameter	OSCIN divide by 2;min/max	OSCIN divide by 1; min/max	Value		Unit
				min	max	
T_{low}	Pulse Width			1.5 INTCLK		ns
T_{high}	Pulse Distance					ns
T_{ext}	Period/fast Mode			78+1 INTCLK		µs
T_{str}	Start Conversion Delay			0.5	1.5	INTCLK
Core Clock issued by Timing Controller						
T_{low}	Pulse Width					ns
T_{high}	Pulse Distance					ns
T_{ext}	Period/fast Mode					µs
T_{str}	Start Conversion Delay					ns

A/D CONVERTER. ANALOG PARAMETERS TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified)

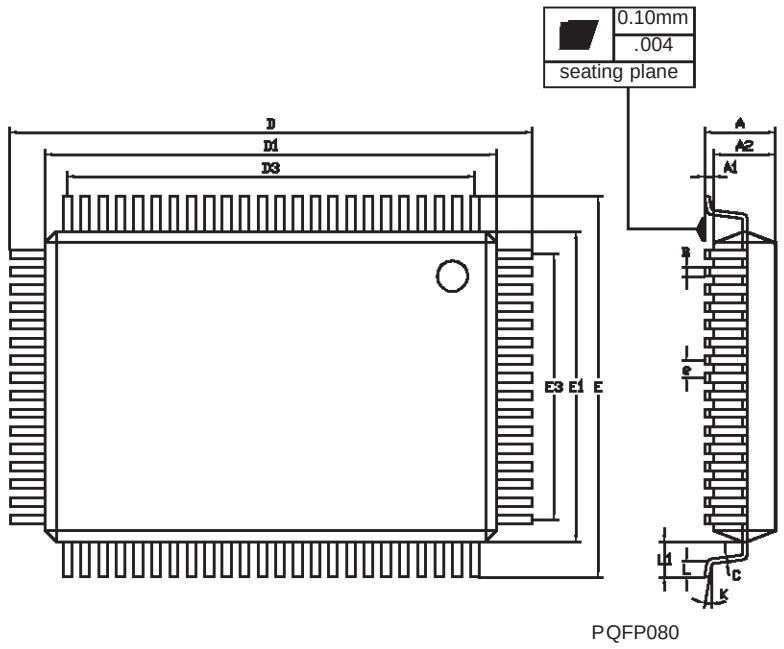
Parameter	Value			Unit	Note
	typ (*)	min	max	(**)	
Analog Input Range		V_{SS}	V_{DD}	V	
Conversion Time Fast/Slow		78/138		INTCLK	(1,2)
Sample Time Fast/Slow		51.5/87.5		INTCLK	(1)
Power-up Time		60		µs	
Resolution	8			bits	
Differential Non Linearity	1.5		2.5	LSBs	(4)
Integral Non Linearity	2		3	LSBs	(4)
Absolute Accuracy	2		3	LSBs	(4)
Input Resistance			1.5	Kohm	(3)
Hold Capacitance			1.92	pF	

Notes: (*) The values are expected at 25 Celsius degrees with V_{DD}= 5V
(**) 'LSBs' , as used here, as a value of V_{DD}/256
(1) @ 24 MHz external clock
(2) including Sample time
(3) it must be considered as the on-chip series resistance before the sampling capacitor
(4) DNL ERROR= max {[V(i) -V(i-1)] / LSB-1} INL ERROR= max {[V(i) -V(0)] / LSB-i}
ABSOLUTE ACCURACY= overall max conversion error

3 GENERAL INFORMATION

3.1 PACKAGE MECHANICAL DATA

Figure 5. 80-Pin Plastic Quad Flat Package



PQFP080

Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.40			0.724	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.80			0.031	
K	0°		7°			
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
	Number of Pins					
N	80		ND	24	NE	16

3.2 ORDERING INFORMATION

Sales Type	OSD	Temperature Range	Package
ST92R195B9Q1	50/60 or 100/120 Hz	0-70°C	PQFP80

Notes: